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| EXAMINER |
|---|
| MAKHDOOM, SAMARINA |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | |

DATE MAILED: 02/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/378,596 | Applicant(s) GUPTA ET AL. |
|---|---|---|
| | Examiner Samarina Makhdoom | Art Unit 2123 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12/11/2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

***Response to Amendment***

1. No Claims are amended.

***Response to Arguments***

2. Applicant's arguments filed 12/11/02 have been fully considered but they are not persuasive with respect to Dey et al; however, the arguments are persuasive with respect to rejection over Abbot.

In the remarks, applicant argues in substance that neither Dey et al nor Abbot teach (1) determining mutually exclusive operations from the specified processor operations based on the desired instruction level parallelism; (2) programmatically assigning instances of functional units from a macrocell library to the sets of mutually exclusive operations, such that each specified operation is associated with a corresponding functional unit; (3) determining how to share a register port for two or more functional unit ports based on the specification of instruction level parallelism among the operations

3. As to arguments (1) – (3), (1) the examiner respectfully disagrees, see Figure 2b, and text in Col. 9, line 20-30, the Figure 2b shows a processor that executes add and multiply instructions in parallel. The operands for the add instructions and multiply instructions are independent of each other making the addition and multiplication operations mutually exclusive (See Col. 4, lines 25-47 where each register is associated with one execution unit). Although Dey uses his processor for a different purpose, it is functionally equivalent to the applicant's invention. (2) See Figure 2b for the multiplier and adder serving as functional units. Also see Figure 1a and text in Col. 6, lines 14-50.

Dey teaches using behavior description or programs to synthesize the system. The execution units or functional units can be adders, multipliers, ALU's, or transfer units. So the program is used to select or assign the function of the functional unit. The operands for the adder and multiplier are independent of each other or mutually exclusive (See Col. 4, lines 25-47 where each register is associated with one execution or functional unit). (3) See Col. 4, lines 25-47 where each register is associated with one execution unit. Dey also discloses that "Although the present invention is described in conjunction with the dedicated register file model, it will be apparent to those skilled in the art that the non-scan DFT methods can be easily modified to be applicable to any arbitrary hardware model." Register ports are inherent to the register file and this design can work with a dedicated register file or another arbitrary hardware model such as one with a shared register file.

Arguments with respect to Abbot have been noted and the rejection over abbot is now withdrawn.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**5. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Dey et al. U.S. Patent No. 5,513,123.**

As per Claims 1 and 9, Dey et al. disclose a method for automatic design of a processor datapath from an input specification including a register file specification, a set of specified processor operations and a desired instruction level parallelism among the specified operations, the method comprising:

determining sets of mutually exclusive operations from the specified processor operations based on the desired instruction level parallelism (See Figure 1a, and text on Col. 6 lines 14-50, the figure displays the parallelism of processor operations through the adder and multiplier units);

programmatically assigning instances of functional units from a macrocell library to the sets of mutually exclusive operations, such that each specified operation is associated with a corresponding functional unit (See Figure 1, and text on Col. 6 lines 14-50 on characteristics of the data paths. The text discloses the specified operations associated with of adders, multipliers, or functional units);

programmatically determining a resource allocation of register file ports to ports of the functional units; and programmatically synthesizing register files with the allocated read/write ports and interconnects between the functional units and the allocated read/write ports (See Col. 9, lines 55-65 for register files receiving data and sending data. The act of receiving and sending data is equivalent to the read/write function, and read/write ports are inherent to a register file).

As per Claim 2, Dey et al. disclose the ports of the functional units each have a corresponding register file port request and programmatically determining the resource allocation includes: programmatically allocating a minimum number of read/write ports that satisfies all of the port requests (See Col. 4, lines 20-25 discuss using an approach

that minimizes hardware to view all datapath loops. Also See Col. 9, lines 55-65 for register files that receive and send data from a particular Execution unit (or ALU or functional unit) therefore programmatically allocating resources).

As per Claim 3, Dey et al. disclose the specification of parallelism among operations is specified as exclusion relationships among operations that indicate which operations cannot be executed concurrently (See Col. 3, lines 36-46, discussing the execution units and the dependencies between the execution units. These dependencies will determine what operations can execute concurrently).

As per Claim 4, Dey et al. disclose the input specification further includes: a mapping between the specified operations and register file types in the register file specification; and operation formats describing inputs and outputs of the specified operations (See Col. 9. lines 41-54 to see organization of register files and the disclosure of controllability points to the register files so they are associated with a particular execution unit or functional unit).

As per Claim 5, Dey et al. disclose the synthesized functional units include macrocell instances, the synthesized register files include register file instances, and the interconnect includes macrocell instances of wires, buses, muxes, or tri-states (See Figure 1a, and corresponding text Col. 6, lines 20-29 showing interconnects of macrocell instances such as buses, wires, adders, and multipliers).

As per Claim 6, Dey et al. disclose determining sets of mutually exclusive operations includes: finding maximal cliques of mutually exclusive operations based on exclusion relations derived from the input specification (See Col. 9, lines 58-65 for the

used of cliques based on the self-looping registers. The larger the number of self-looping registers, the larger the clique).

As per Claim 7, Dey et al. disclose synthesizing functional units includes: building a list of valid functional units based on opcodes and latency of the specified operations (See Figure 1a. and text on Col. 6, lines 14-50, a list of valid functions are displayed in this figure and Table I);

from the list, selecting functional units such that each functional unit covers a maximum number of operations in a set of mutually exclusive operations (See Figure 1a, and corresponding text Col. 6, lines 20-29 showing interconnects i.e. buses, adders, and multipliers; the connections shown on Figure 1a allow to the system to perform different operations simultaneously covering the maximum number of operations).

As per Claim 8, Dey et al. disclose using the instruction level parallelism from the input specification to identify which functional unit ports can be allocated to the same register port, and allocating selected functional unit ports to a single, shared register port (See Col. 9, lines 31-54 showing the different inputs and outputs (or ports) of the register files and the use of test pins as test 'ports'. Furthermore, the output of functional unit A2 is multiplexed with the test points to ensure the functionality of the datapath remains unchanged. The same register file ports of RA2 and LA2 are associated with the functional unit port of A2).

As per Claims 10 and 15, Dey et al. disclose a method for automatic synthesis of functional units in a programmable processor datapath, the method comprising:

from an input specification defining a set of specified processor operations and instruction level parallelism among the specified operations, determining sets of mutually

exclusive operations (See Figure 1a, and text in Col. 6 lines 14-50 for the parallelism of the adder and multiplier operations);

programmatically assigning instances of functional units from a macrocell library to the sets of mutually exclusive operations, such that each specified operation is associated with a corresponding functional unit (See Figure 1a, and text in Col. 6 lines 14-50 for the parallelism of the adder and multiplier operations, the add function is associated with the adder functional unit and the multiply function is associated with the multiply functional unit);

and programmatically synthesizing the functional units from the macrocell library such that the functional units are described in a hardware description language (See Col. 2, lines 44-66 for the used of hardware description languages such as RTL to define and test a circuit).

As per Claim 11, Dey et al. disclose determining sets of mutually exclusive operations includes: finding exclusion cliques where each clique represents a maximal set of mutually exclusive operations; and wherein assigning instances of functional units includes programmatically selecting instances of functional units to cover the cliques from the macrocell library (See Col. 9, lines 55 to 62 for the use of register cliques, each set of registers such as RA2 or RA1 as assigned to a functional unit).

As per Claim 12, Dey et al. disclose synthesizing functional units includes: building a list of valid functional units based on opcodes of the specified operations; from the list, selecting functional units such that each functional unit covers a maximum number of operations in a set of mutually exclusive operations (See Col. 15, lines 63-67,

where Dey et al. disclose maximizing control and observation points for the datapath, this same method could be applied to datapath functional units and opcodes).

As per Claim 13, Dey et al. disclose functional unit instances are assigned such that the semiconductor area covered by functional units in the processor design is minimized (The design goal to minimize semiconductor area is inherent to the semiconductor art).

As per Claim 14, Dey et al. disclose the functional unit instances are assigned such that the number of operations covered by each of the functional unit instances is maximized (See Col. 15, lines 63-67, where Dey et al. disclose maximizing control and observation points for the datapath, this same method could be applied to datapath functional units, parallelism, and opcodes).

As per Claim 16 and 18, Dey et al. disclose a method for automatic synthesis of a register file and functional unit-register file interconnect in a processor, based on an input specification of register file types in the processor, specified processor operations, desired instruction level parallelism among the specified operations and functional units in the processor, the method comprising:

for each type of register file specified in the processor, establishing a set of read/write port requests between the functional units and each of the register file types (See Col. 4, lines 20-25 discuss using an approach that minimizes hardware to view all datapath loops. Also See Col. 9, lines 55-65 for register files that receive and send data from a particular Execution unit (or ALU or functional unit) therefore programmatically allocating resources);

programmatically computing a resource allocation of register ports in the register file types to read/write port requests, including determining how to share a register port for two or more functional unit ports based on the specification of instruction level parallelism among the operations and (See Col. 4, lines 20-25 discuss using an approach that minimizes hardware to view all datapath loops. Also See Col. 9, lines 55-65 for register files that receive and send data from a particular Execution unit (or ALU or functional unit) therefore programmatically allocating resources);

programmatically synthesizing register files with the allocated read/write ports and interconnects between the functional units and the allocated read/write ports. (See Col. 9, lines 55-65 for register files receiving data and sending data The sending and receiving data function are equivalent to the read/write function and an apparatus for reading/writing such as ports are inherent to a register file).

As per Claim 17, Dey et al. disclose the resource allocation uses a contiguous allocation heuristic that simplifies interconnect layout by allocating register port requests from a functional unit to contiguous register ports (See Col. 6, lines 14-30 for datapath layout and Figure 1a for register port and functional unit connections).

***Conclusion***

10. 6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS

ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samarina Makhdoom whose telephone number is 703-305-7209. The examiner can normally be reached on Part Time on Friday, and Sunday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J. Teska can be reached on 703-305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0040 for regular communications and 703-305-0040 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

SM
February 3, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER